REMARKS

Applicant thanks the Examiner for the thorough examination of the application. This paper is filed in responsive to the Office Action dated September, 11, 2007.

Present Status of Application

Claim 29 is rejected under 35 U.S.C. 102(e) as being anticipated by Na et al.(US 5,942,767). Claims 33 and 35 are rejected under 35 U.S.C. 102(b) being anticipated by Shimada et al.(US 5,726,461). Claims 31 and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Na et al.(US 5,942,767) in view of Kaneko (US 6,433,842).

Detailed discussion about amendment to the claims

In this paper, claims 29 and 33 are amended. Support for the amended claim 29 can be found, for example, in FIG. 2F of the application, which discloses, by way of example and not of limitation, that "*the first sacrifice layer* (e.g. element 29 on the left) *is only formed on a portion of a doped silicon layer* (e.g. element 25), *chosen between the source doped silicon layer* (e.g. element 25) *and the drain doped silicon layer* (e.g. element 25), *and the respective source* (e.g. element 26a) *or drain electrode* (e.g. element 26b) *directly contacts a portion of the doped silicon layer* (e.g. element 25) *not covered by the respective first sacrifice layer* (e.g. element 29 on the left) *or second sacrifice layer* (e.g. element 29 on the right)."

Support for the amended claim 33 can be found, for example, in FIG. 4F of the application, which discloses, by way of example and not of limitation, that "*wherein the first sacrifice layer* (e.g. element 49 on the left) *is only disposed below a portion of a doped silicon layer* (e.g. element 45) *chosen between the source doped silicon layer* (e.g.

element 45), *and the drain doped silicon layer* (e.g. element 45), *and the respective source doped silicon layer* (e.g. element 45) *or drain doped silicon layer* (e.g. element 45) *directly contacts a portion of the semiconductor layer* (e.g. element 44)."

Rejections Under 35 U.S.C. 102(e)

Claim 29 is rejected under 35 U.S.C. 102(e) as being anticipated by Na et al.(US 5,942,767).

A proper rejection of a claim under 35 U.S.C. §102 requires that a single prior art reference disclose each element of the claim. *See, e.g., W.L. Gore & Assoc., Inc. v. Garlock, Inc.*, 721 F.2d 1540, 220 USPQ 303, 313 (Fed. Cir. 1983). Anticipation requires that each and every element of the claimed invention be disclosed in a single prior art reference. *See e.g., In re Paulsen*, 30 F.3d 1475, 31 USPQ 2d 1671 (Fed. Cir. 1994); *In re Spada*, 911 F.2d 705, 15 USPQ 2d 1655 (Fed. Cir. 1990). For anticipation, there must be no difference between the claimed invention and the reference disclosure, as viewed by a person of ordinary skill in the field of the invention. *See, e.g., Scripps Clinic & Res. Found. v. Genentech, Inc.*, 927 F.2d 1565, 18 USPQ 2d 1001 (Fed. Cir. 1991.)

Amended Claim 29 recites in part:

"wherein the first sacrifice layer is only formed on a portion of a doped silicon layer chosen between the source doped silicon layer and the drain doped silicon layer, and the respective source or drain electrode directly contacts a portion of the doped silicon layer not covered by the respective first sacrifice layer or second sacrifice layer."

In the thin film transistor of amended claim 29, the first sacrifice layer is only formed on a portion of the source doped silicon layer, and the source electrode directly contacts a portion of the source doped silicon layer not covered by the first sacrifice layer, or the second sacrifice layer is only formed on a portion of the drain doped silicon layer, and the drain electrode directly contacts a portion of the drain doped silicon layer not covered by the second sacrifice layer.

On page 2 of the office action, the examiner asserts that "Regarding claim 29, Na teaches (Fig. 5f) a thin film transistor, comprising... first and second sacrificial layers (461) with island shapes respectively formed on the source doped silicon layer (441 on the left) and drain doped silicon layer (441 on the right) and formed on the semiconductor layer (16)."

It is noted that the Examiner construes the silicide layer (element 461) in Na as the first and second sacrificial layer of claim 29. However, the silicide layer 461 in Na covers the entire top surface of the amorphous silicon layer 441. Therefore, i) the silicide layer (element 461) is not formed only on a portion of the amorphous silicon layer (element 441), and ii) the source electrode (element 471) does not directly contact a portion of the amorphous silicon layer (element 441) not covered by the silicide layer (element 461) in Na. Applicant submits that Na does not teach "*the first sacrifice layer is only formed on a portion of a doped silicon layer chosen between the source doped silicon layer and the drain doped silicon layer, and the respective source or drain electrode directly contacts a portion of the doped silicon layer not covered by the respective first sacrifice layer or second sacrifice layer*" as recited in amended claim 29. Since Na fails to teach every element as set forth in the claim 29, reconsideration of this rejection is hereby respectfully requested.

Rejections Under 35 U.S.C. 102(b) of claims 33 and 35

Claims 33 and 35 are rejected under 35 U.S.C. 102(b) being anticipated by Shimada et al.(US 5,726,461).

Amended Claim 33 recites in part:

"wherein the first sacrifice layer is only disposed below a portion of a doped silicon layer chosen between the source doped silicon layer and the drain doped silicon layer, and the respective source doped silicon layer or drain doped silicon layer directly contacts a portion of the semiconductor layer."

On pages 3 and 4 of the office action, the examiner assert that "Regarding claim 33, Shimada teaches (fig. 7)...a source doped silicon layer 25 and a drain doped silicon layer (25 on the right hand side) formed above the first sacrifice layer 15, second sacrifice layer (15 on the right hand side), and the semiconductor layer 13...".

It appears that the Examiner construes the micro crystal n+ silicon layer (element 15) in Shimada as the first and second sacrificial layer of claim 33, and the n+ silicon layer (element 25) in Shimada as the doped silicon layer of claim 33. However, the Examiner is respectfully reminded that Shimada teaches patterning the n+ silicon layer (element 25) and the micro crystal n− silicon layer (element 15) at a single step in col. 8, lines 13-17. and the n+ silicon layer (element 25) and the micro crystal n+ silicon layer (element 15) are entirely matched and stacked as shown in, FIG. 4. Reference :Col. 8, lines 13-17 in Shimada "Then, the micro-crystalline n+ silicon layer 15 and the amorphous n+ silicon layer 25 are patterned to form the source electrode 101a and the drain electrode 101b

each having the two-layer structure"

Applicant submits that Shimada does not teach "*wherein the first sacrifice layer is only disposed below a portion a doped silicon layer chosen between the source doped silicon layer and the drain doped silicon layer, and the respective source doped silicon layer or drain doped silicon layer directly contacts a portion of the semiconductor layer*" as recited in amended claim 33.

Since Shimada fails to teach every element as set forth in the claim 33, reconsideration of th s rejection is hereby respectfully requested. Applicant respectfully asserts that claim 33 is allowable over the cited reference. Insofar as claim 35 depends from claim 33, it is the Applicant's belief that claim 35 is also allowable at least by virtue of it's dependency.

Rejections Under 35 U.S.C. 103(a)

Claims 31 and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Na et al.(US 5,942,767) in view of Kaneko (US 6,433,842). For similar reasoning as applied above it is believed that claim 29 is allowable over the cited reference. Insofar as claims 31 and 32 depends from claim 29, it is the Applicant's belief that claim 31 and 32 are also allowable at least by virtue of their dependency.

* * * * *

Conclusion

Applicants respectfully contend that all conditions of patentability are met in the pending application as amended. All amendments herein are made without prejudice. The Examiner is respectfully requested to pass the application to issue.

The Commissioner is authorized to charge any additional fees, which may be required or credit overpayment to deposit account no. 12-0415. In particular, if this response is not timely filed, then the Commissioner is authorized to treat this response as including a petition to extend the time period pursuant to 37 CFR 1.136 (a) requesting an extension of time of the number of months necessary to make this response timely filed and the petition fee due in connection therewith may be charged to deposit account no. 12-0415.

I hereby certify that this correspondence is being facsimile transmitted to the United States Patent and Trademark Office, fax no. (571)-273-8300 on

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